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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,614	09/19/2003	Kazumi Inoh	79001-2037	6405
20999	7590	06/06/2005	EXAMINER	
FROMMER LAWRENCE & HAUG 745 FIFTH AVENUE- 10TH FL. NEW YORK, NY 10151			MANDALA, VICTOR A	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/665,614

Applicant(s)

INOH ET AL.

Examiner

Victor A. Mandala Jr.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 March 2005.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-7,9-12,20,21,23-25 and 27-29 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1,3,4,6,7,9,10,12,20,21,23,24,27 and 28 is/are rejected.
7) ☒ Claim(s) 5,11 and 25 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The Applicant argues that the 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,630,714 Sato et al. does not teach the cavity to be wider than the element region, but the examiner disagrees. Sato et al.'s figure 17 teaches an element region #72, which is the channel region not including the source and drain, but the space between them. The channel region #72 is very clear to be less in width in the given view of figure 17 than the cavity region #71. It is unclear where the Applicant feels that it is not, hence the rejection stands as is and is made final.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 4, and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,630,714 Sato et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

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2. Referring to claim 1, a semiconductor device comprising: a semiconductor substrate, (Figure 17 #60); flat-plate-shaped cavity, (Figure 17 #71), made in the semiconductor substrate, (Figure 17 #60); and an element isolating region, (Figure 17 #73), formed in the surface of the semiconductor substrate, (Figure 17 #60), and located at the sides the cavity, (Figure 17 #71), the cavity being wider than an element region, (Figure 17 #72 the channel), provided on the cavity, (Figure 17 #71).
3. Referring to claim 3, a semiconductor device, wherein the element isolating region, (Figure 17 #73), and the cavity, (Figure 17 #71,) enclose the element region, (Figure 17 #72 the channel), and electrically separate the element region, (Figure 17 #72 the channel), from the semiconductor substrate, (Figure 17 #60).
4. Referring to claim 4, a semiconductor device, wherein only one element region, (Figure 17 #72 the channel), provided on the cavity, (Figure 17 #71).
5. Referring to claim 6, a semiconductor device, wherein the element isolating region, (Figure 17 #73), is formed of an oxide film, (STI formation Col. 13 Lines 58-64), obtained by oxidizing the semiconductor substrate, (Figure 17 #60).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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Claims 1, 3, 4, 6, 7, 9, 10, 12, 20, 21, 23, 24, 27, & 28 are rejected under 35

U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication No. 2003/0151112

Yamada et al.

6. Referring to claim 1, a semiconductor device comprising: a semiconductor substrate, (Figure 10A & C #10); flat-plate-shaped cavity, (Figure 10A & C #40), made in the semiconductor substrate, (Figure 10A & C #10); and an element isolating region, (Figure 10A & C #STI), formed in the surface of the semiconductor substrate, (Figure 10A & C #10), and located at the sides the cavity, (Figure 10A & C #40), the cavity, (Figure 10A & C #40), being wider than an element region, (Figure 10A & C #12 the channel), provided on the cavity, (Figure 10A & C #40).

7. Referring to claim 3, a semiconductor device, wherein the element isolating region, (Figure 10A & C #STI), and the cavity, (Figure 10A & C #40), enclose the element region, (Figure 10A & C #12), and electrically separate the element region, (Figure 10A & C #12 the channel), from the semiconductor substrate, (Figure 10A & C #10).

8. Referring to claim 4, a semiconductor device, wherein only one element region, (Figure 10A & C #12 the channel), provided on the cavity, (Figure 10A & C #40).

9. Referring to claim 6, a semiconductor device, wherein the element isolating region, (Figure 10A & C #STI), is formed of an oxide film, (STI formation), obtained by oxidizing the semiconductor substrate, (Figure 10A #10).

10. Referring to claim 7, a semiconductor device comprising: a semiconductor substrate, (Figure 10A, B, & C #10); a plurality of flat-plate-shaped cavities, (Figure 10A, B, & C #40), made in the semiconductor substrate, (Figure 10A, B, & C #10); and an element isolating region,

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(Figure 10A, B, & C #STI), formed in the surface of the semiconductor substrate, (Figure 10A, B, & C #10), between adjacent ones of the cavities, (Figure 10A, B, & C #40), a part of the element isolating region, (Figure 10A, B, & C #STI), being exposed to the cavities, (Figure 10A, B, & C #40), each cavity, (Figure 10A, B, & C #40), being wider than each element region, (Figure 10A, B, & C #41 & 12 the channel), provided on each cavity, (Figure 10A, B, & C #40), respectively.

11. Referring to claim 9, a semiconductor device, wherein the element isolating region, (Figure 10A, B, & C #STI), and the cavities, (Figure 10A, B, & C #40), enclose the element regions, (Figure 10A, B, & C #41 & 12 the channel), and electrically separate the element regions, (Figure 10A, B, & C #41 & 12 the channel), from the semiconductor substrate, (Figure 10A, B, & C #10).

12. Referring to claim 10, a semiconductor device, wherein only one element region, (Figure 10A, B, & C #41 & 12 the channel), is provided on the cavity, (Figure 10A, B, & C #40).

13. Referring to claim 12, a semiconductor device, wherein the element isolating region, (Figure 10A, B, & C #STI), is formed of an oxide film, (STI), obtained by oxidizing the semiconductor substrate, (Figure 10A, B, & C #40).

14. Referring to claim 20, a method of fabricating a semiconductor device, comprising: making flat-plate-shaped cavities partly a semiconductor substrate, (Figure 10A, B, & C #10); forming an insulating film, (Figure 10A, B, & C #STI), in the surface of the semiconductor substrate, (Figure 10A, B, & C #10), between adjacent ones of the cavities, (Figure 10A, B, & C #40), in such a manner that a part of the insulating film, (Figure 10A, B, & C #STI), is exposed to the cavities, (Figure 10A, B, & C #40), so as to electrically separate element regions, (Figure

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10A, B, & C #41 & 12 the channel), provided on the cavities, (Figure 10A, B, & C #40), from each other; each cavity, (Figure 10A, B, & C #40), being wider than each element region, (Figure 10A, B, & C #41 & 12 the channel); and forming semiconductor elements, (Figure 10A, B, & C #14u&v, 15u&v, and 16u&v), on the element regions, (Figure 10A, B, & C #41 & 12 the channel).

15. Referring to claim 21, a method of fabricating a semiconductor device, wherein the insulating film, (Figure 10A, B, & C #STI), is formed by oxidizing, (STI), the surface of the semiconductor substrate, (Figure 10A, B, & C #10).

16. Referring to claim 23, a method of fabricating a semiconductor device, wherein the insulating film, (Figure 10A, B, & C #STI), and the cavities, (Figure 10A, B, & C #40), enclose the element regions, (Figure 10A, B, & C #41 & 12 the channel), and electrically separate the element regions, (Figure 10A, B, & C #41 & 12 the channel), from the semiconductor substrate, (Figure 10A, B, & C #10).

17. Referring to claim 24, a method of fabricating a semiconductor device, wherein only one element region, (Figure 10A, B, & C #41 & 12 the channel), provided on each of the cavities, (Figure 10A, B, & C #40).

18. Referring to claim 27, a semiconductor device, wherein the cavity, (Figure 10A, B, & C #40), has no element therein.

19. Referring to claim 28, a semiconductor device, wherein the cavity, (Figure 10A, B, & C #40), has no element therein.

20. Referring to claim 29, a semiconductor device, wherein the cavity, (Figure 10A, B, & C #40), has no element therein.

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Allowable Subject Matter

21. Claims 5, 11, 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A. Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
5/25/05

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